**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-20. (Canceled).

21 (New). A non-volatile semiconductor memory device, comprising:

a memory cell array having non-volatile memory cells arranged therein, in which initial set-up data are stored;

data latch circuits configured to hold said initial set-up data read out from said memory cell array;

a controller configured to control operations of said memory cell array; and

a clock generator configured to generate a clock signal that is used to define an operation timing of said controller, wherein

said controller is so programmed as to read out a clock cycle adjustment data within said initial set-up data in the beginning after power-on, thereby adjusting a clock cycle of said clock signal output from said clock generator by use of said clock cycle adjustment data, and then read out the remaining initial set-up data by use of the adjusted clock signal.

22 (New). The memory device according to claim 21, wherein

the remaining initial set-up data contain defective address data, control data used for controlling memory operations and code data.

23 (New). The memory device according to claim 21, further comprising

a ready/busy signal circuit configured to output a busy signal during said initial set-up data are read out from said memory cell array and transferred to said data latch circuits.

24 (New). The memory device according to claim 21, further comprising:

a power-on detecting circuit configured to detect power-on so as to activate said controller for performing data read out operation of said initial set-up data stored in said memory cell array.

25 (New). The memory device according to claim 21, wherein said clock generator comprises:

a ring oscillator; and

a delay circuit disposed in said ring oscillator, a delay time of which being defined by said clock cycle adjustment data.

26 (New). The memory device according to claim 25, wherein

said delay circuit comprises a CR time constant circuit having a resistor and a capacitor, at least one of which is variably controlled in response to said clock cycle adjustment data.

27 (New). The memory device according to claim 21, further comprising:

a boost circuit configured to boost a power supply voltage in response to power-on so as to supply a boosted voltage to a power supply node of said clock generator.

28 (New). The memory device according to claim 21, wherein

said controller has a test mode so programmed as to check and rewrite said initial set-up data stored in at least one of said memory cell array and said data latch circuits on receipt of a command input from an external terminal.

29 (New). The memory device according to claim 21, wherein

said memory cell array has a plurality of NAND cell units each of which has a plurality of serially connected memory cells and a select transistor through which said serially connected memory cells are connected to a bit line, said serially connected memory cells being driven by different word lines from each other.

30 (New). A non-volatile semiconductor memory device, comprising:

a memory cell array having non-volatile memory cells arranged therein, in which initial set-up data are stored;

data latch circuits configured to hold said initial set-up data read out from said memory cell array;

a controller configured to control operations of said memory cell array;

a clock generator configured to generate a clock signal that is used to define an operation timing of said controller;

a first boost circuit configured to output a boosted voltage necessary for data read, program and erase of said memory cell array; and

a second boost circuit configured to boost a power supply voltage in response to power-on so as to supply a boosted voltage to a power supply node of said clock generator.

31 (New). The memory device according to claim 30, wherein

said controller is so programmed as to read out a clock cycle adjustment data within said initial set-up data stored in said memory cell array in the beginning after power-on, thereby adjusting said clock cycle of said clock signal output from said clock generator by use of said clock cycle adjusting data, and then read out the remaining initial set-up data by use of the adjusted clock signal.

32 (New). The memory device according to claim 31, wherein

the remaining initial set-up data contain defective address data, control data used for controlling memory operations and code data.

33 (New). The memory device according to claim 31, further comprising

a ready/busy signal circuit configured to output a busy signal during said initial set-up data are read out from said memory cell array and transferred to said data latch circuits.

34 (New). The memory device according to claim 31, further comprising:

a power-on detecting circuit configured to detect power-on so as to activate said controller for performing data read out operation of said initial set-up data stored in said memory cell array.

35 (New). The memory device according to claim 30, wherein

said clock generator comprises:

a ring oscillator; and

a delay circuit disposed in said ring oscillator, a delay time of which being defined by said clock cycle adjustment data.

36 (New). The memory device according to claim 35, wherein

said delay circuit comprises a CR time constant circuit having a resistor and a capacitor, at least one of which is variably controlled in response to said clock cycle adjustment data.

37 (New). The memory device according to claim 30, wherein

said controller has a test mode so programmed as to check and rewrite said initial set-up data stored in at least one of said memory cell array and said data latch circuits on receipt of a command input from an external terminal.

38 (New). The memory device according to claim 30, wherein

said memory cell array has a plurality of NAND cell units each of which has a plurality of serially connected memory cells and a select transistor through which said serially connected memory cells are connected to a bit line, said serially connected memory cells being driven by different word lines from each other.